MT ALU Assignment

ECE 3561, 12/04/19

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***Alu Code Listing***

**LIBRARY IEEE;**

**USE IEEE.STD\_LOGIC\_1164.ALL;**

**ENTITY alu IS**

**PORT (a,b : IN std\_logic\_vector (15 downto 0);**

**cin,arlo : IN std\_logic;**

**ltt : std\_logic\_vector(0 to 3);**

**res : OUT std\_logic\_vector (15 downto 0);**

**cout : OUT std\_logic);**

**END alu;**

**ARCHITECTURE one OF alu IS**

**COMPONENT mux2\_to\_1x16 IS**

**PORT (a,b : IN std\_logic\_vector(15 downto 0);**

**sa,sb : IN std\_logic;**

**muxout : OUT std\_logic\_vector(15 downto 0));**

**END COMPONENT;**

**COMPONENT log16 IS**

**PORT(a,b : IN std\_logic\_vector(15 downto 0);**

**res : OUT std\_logic\_vector(15 downto 0);**

**ltt : IN std\_logic\_vector(0 to 3));**

**END COMPONENT;**

**COMPONENT add16 IS**

**PORT (a,b : IN std\_logic\_vector (15 downto 0);**

**cin : IN std\_logic;**

**sum : OUT std\_logic\_vector (15 downto 0);**

**cout : OUT std\_logic);**

**END COMPONENT;**

**SIGNAL lu\_result,addr\_result : std\_logic\_vector (15 downto 0);**

**SIGNAL notArlo : std\_logic;**

**BEGIN**

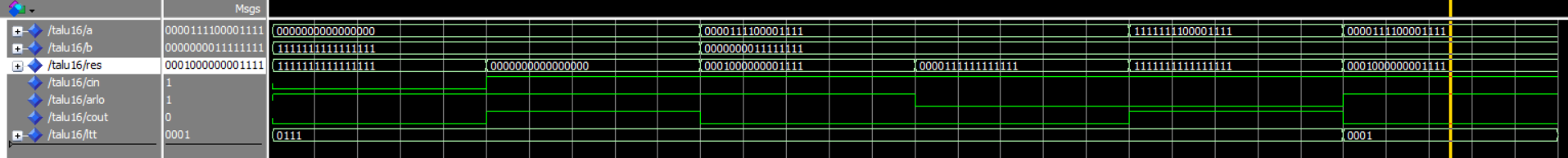
**logicUnit0 : log16 PORT MAP(a,b,lu\_result,ltt);**

**addr0 : add16 PORT MAP(a,b,cin,addr\_result,cout);**

**mux0 : mux2\_to\_1x16 PORT MAP(addr\_result,lu\_result,arlo,notArlo,res);**

**notArlo <= not(arlo);**

**END one;**

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